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Abstract

The present invention relates to a device and a fabricating method thereof, the device having a gate hole of triode structure fabricated by using an anode oxidation process, which can be operated by a very low driving voltage and emit electrons in a constant density. The fabricating method of a gate hole in accordance with the present invention includes the steps of: depositing an insulating layer and a metal layer on a substrate; forming a plurality of microholes in the metal layer by performing an anode oxidation process on the metal layer; and forming a plurality of insulating holes on the insulating layer by etching a part of the insulating layer, which is exposed through the microholes of the metal layer, by using the processed metal layer as a mask. A field emission device of the present invention includes: a lower substrate having an insulating layer and a metal layer deposited thereon, a plurality of microholes formed in the insulating layer and the metal layer by using an anode oxidation process and photo-etching method, emitters for emitting electrons formed in the microholes and gate electrodes for obtaining the electrons emitted from the emitters; a upper substrate having a transparent electrode and a fluorescent body; and a spacer for maintaining a vacuum gap in the upper and lower substrates, which is formed on the upper substrate.

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Submit Report

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Patent Application

Right Classification	Patent.
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Submission Date	2000.11.28
Korean Title of Invention	Gate Hole Fabricating Method Thereof, and Fabricating Method Thereof
English Title of Invention	Gate Hole Fabricating Method Thereof, and Fabricating Method Thereof

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Request for Examination Demand.

Purport

We file an application under Article 42 of Patent Act, file a Request for Examination under Article 60 of Agent Yeong-Ho Kim (Signature)

Official Fee

Application Fee	20 page(s) 29,000 won.
Additional Application Fee	1,000 one-sided a won.
Priority Fee	0 case 0 won.
Examination Fee	12 claim(s) 493,000 won.
Total	523,000 won.

Attached Documents

1. 1 summary · specification(drawing).

Patent Specification

Abstract

Abstract

The present invention is to provide the new device in which it makes the driving voltage which is quite triode structure of the gate hole using the anodic oxidation process and the uniform electron emission p method of manufacture thereof.

The method of manufacturing a gate hole of the present invention is equipped with the step laminating t layer and metal layer onto the top of the substrate, the step oxidizing the metal layer and forms a plural within the metal layer, and the step that forms a cavity on the insulating layer by having the anodic oxid pattern to a mask and removing the insulating layer between the metal pattern.

The field emission device of the present invention is equipped with a plurality of fine holes which is fori anodizing and photo etching it laminates the insulating layer and metal layer onto the top of the substrat which emits the electronics it is positioned within the fine hole and the lower plate including the gate el out the electronics from an emitter and the upper plate, including the transparent electrode and fluoresc and the spacer which maintains the vacuum gap of the lower plate and top it is formed on the upper plat

Representative Drawing

Drawing 8

Specification

Title of Invention

Gate Hole Fabricating Method Thereof, Field Emission Display and Fabricating Method Thereof{Gate H Method Thereof, Field Emission Display and Fabricating Method Thereof}

Brief Description of the Drawings

Figure 1 is a cross-sectional view showing the conventional three pole CNT field emission device.

Figs. 2a through 2d are the cross-sectional view showing a stepwise the manufacturing method of the C emission device illustrated in Figure 1.

Figure 3 is a cross-sectional view showing the method of manufacturing a gate hole of the field emissio puntiform according to the embodiment of the present invention.

Figure 4 is a cross-sectional view showing the manufacturing method of the field emission device inclu illustrated in Figure 3.

Figs. 5a through 5c is a drawing showing the embodiment forming the electric field emission part illustr.

Figure 6 is a schematical diagram of a pixel illustrated in Figure 5.

Figure 7 is a cross-sectional view of the pixel which steals in fig. 6 according to the line "A-A'" and sh

Figure 8 is a drawing showing the field emission device of a triode illustrated in Figure 5.

<The description of reference numerals of the main elements in drawings>

10,64: lower plate 11:lower conduction electrode(cathode electrode)

12,66: insulating layer 13,65:upper conductivity book on sex pole(gate electrode)

14: aluminum foil 15: anode oxidation layer.

16: catalyzing transition metal 17: carbon nanotube.

18: photo-resistor 19: resistant layer.

20: spacer 21: anode electrode.

22,62: fluorescent substance 23,63: emitter.

24,68: gate hole 25,69: cavity.

27,60: upper plate 65a: gate metal layer.

66a: insulating material layer 70: cathode.

The Detailed Description of Invention

The Purpose of Invention

Field of Invention and the Prior Art

The present invention relates to the manufacturing method and field emission device of the gate hole and manufacture thereof, particularly, to the manufacturing method of the super minute gate hole using the an process and the field emission device making the low driving voltage and the uniform electron emission p method of manufacture thereof.

Recently, as to the carbon nanotube (it says to be "CNT" less than the Carbon Nanotube) highlighted as tl in the number nm, with having the crystalline structure of the quite small diameter of the several tens nm resistance characteristic and the mechanical strength are excellent and the of which application is expect manufacture of the field emission device using CNT is studied as one field of application. Especially, the a field emission display is expected. , in addition this can lower the driving voltage than this uses the field e including the existing spint type tip or the silicon tip etc. since it can lower the electron emission voltage CNT as the field emission device the element fabrication in which the chemical resistance characteristic a mechanical strength of CNT are excellent and the reliability is good is due to be possible. As to the reasc

electric field radiation voltage of CNT is low, the turn-on field in which a diameter is quite small to a nm enhancement factor is big and the electron emission occurs is due to be lower than 1~5V / ㎛.

Figure 1 shows the conventional triode structure CNT field emission device.

Referring to Figure 1, the conventional triode structure CNT field emission device provides the fluoresce on the gate electrode (65), on the CNT emitter (63) on the cathode (70), on the lower plate (64) and cath insulating layer (66), and insulating layer (66) and upper plate (60). In this field emission device, the elect with the voltage applied between the cathode (70) and gate electrode (65) in the CNT emitter. The emitte accelerated with the anode (not illustrated) on the upper plate (60) and the electronics collides the electr fluorescent substance (62). In this case, the quantity of emission is controlled with the voltage applied in (65).

The figs. 2a through 2d gradually,by stages shows the manufacturing method of the CNT field emission d in Figure 1.

As shown in Figure 2a, the cathode (70), the insulating material layer (66a) and gate metal layer (65a) are become on the lower plate (64) with the deposition Haage. Subsequently, the gate electrode (65) which a 2b, is formed with the gate hole (68) as the by etching the gate metal layer (65a), is prepared for. The ins layer (66a) is etched through the next, and the hole (68) of the gate electrode (65) and the insulating laye shown in Figure 2c, the cavity (69) is formed is prepared for. And CNT is grown on the cathode (70) exp gate hole (68) and cavity (69) and as shown in Figure 2d, the CNT emitter (63) is formed.

Recently, as to the field emission device of the microtip type, efforts of lowering the driving voltage had l performed. In order to achieve the efficient field concentration and the low driving voltage, as it is near a the team pointed end and the gate hole, it is advantageous for the team pointed end. Therefore, it is nece process develop in which the reliability and large area are possible while reducing the size of the gate ho is necessary to have the new additional equipment and it is considerably the gate hole size up to date con sub micron (sub-micron) in case of methods canning be formed with eutectic phase.

Moreover, as to the emitting device using the conventional carbon nanotube, , in addition it is difficult to all nanotubes in case of growing in the top of the substrate to the random direction or coating in the scre process of being new for the vertical alignment has to be developed. Moreover, in case the distance of th nanotube and gate electrode is not fixed, the distance has the disadvantage that it cannot become the fiel similar on the whole, in case that is, the length of manufactured carbon nanotubes is not uniform.

Technical Problems to be solved by the Invention

Therefore, an object of the present invention is to provide the manufacturing process of the gate hole mi anodic oxidation process.

And by using the super minute gate hole, the field emission device can operate to the low power is provi electric field can be efficiently focused by using the carbon nanotube. The manufacturing process which manufacture the carbo nanotube of the constant height through the former specimen is provided.

The Structure and Function of the Invention(Device)

To accomplish the above objects, the method of manufacturing a gate hole of the present invention is e step laminating the insulating layer and metal layer onto the top of the substrate, the step oxidizing the forms a plurality of fine holes within the metal layer, and the step that forms a cavity on the insulating l the anodic oxidized metal pattern to a mask and removing the insulating layer between the metal patter

To accomplish the above objects, the field emission device of the present invention is equipped with a p holes which is formed with an anodizing and photo etching it laminates the insulating layer and metal la the substrate and the emitter which emits the electronics it is positioned within the fine hole and the lo the gate electrode drawing out the electronics from an emitter and the upper plate, including the transp and fluorescent substance and the spacer which maintains the vacuum gap of the lower plate and top it upper plate done.

Another object of the present invention and features are clearly found besides a purpose through the de the embodiment referring to the attached view.

Referring to figs. 3 through 8, it afterward decides to illustrate for the desirable embodiment of the pre

Figs. 3a through 3d are the cross-sectional view showing the gate hole forming process according to th the present invention.

As shown in Figure 3a, siO2 the insulating layer (12) is deposited on the top of the silicon (Si) wafer or substrates (10) to a method including the radio frequency magnetron sputtering (rf magnetron sputterin vapor method etc. to 0.1~1㎛ thickness. The aluminum foil (14) is weighed with the series processing w frequency or the direct current magnetron sputtering (rf or dc magnetron sputtering), the vacuum depos with 0.1~0.5㎛ thickness with the deposition heartburnings. Here, it may be acceptable that in case of tl substrates (10), when being advantageous for the fine hole (24) formation and depositing the insulating nitride system which is not oxide system is used to have the surface roughness of about silicon wafer.

As shown in Figure 3b, as to the anode oxidation layer (15), the nanohole (24) which has the diameter o deciding on the specimen in which the aluminium (Al) is evaporated among the phosphoric acid or the o: to an anode and the platinum to the opposite cathode and adding the direct current voltage of about 30~ ends and the aluminium (Al) being oxidized and consisting of the alumina (Al2O3) used as the hard mask is, a nanohole is formed owing to an anodizing.

As shown in Figure 3c, it has the anodic oxidized alumina (15) as the hard mask and if the anisotropic r etching (it says to be "RIE" less than reactive ion etching :) is performed under the mixed gas atmosphe CHF3, the insulating layer hole (cavity) (25) of the vertical direction is formed with SiO2 as the about a is, the cavity (25) is formed owing to the photo etching.

As shown in Figure 3d, if the alumina is performed a wet etching and it removes, the cavity (25) is form this cavity (25) coincides with the size of the anodic oxidized alumina fine hole (24).

Figs. 4a through 4g are the cross-sectional view showing 3 electrode structure of the present invention

As shown in Figure 4a, the cr, nb, mo, W etc which is the refractory metal is used on the glass substrat bottom electrode (11). The Nb standing well in HTO is deposited by the radio frequency magnetron spu magnetron sputtering) to about 1000Å thickness. The duplex film which deposits Cr with about 50~100 terminate an etching in RIE of the SiO2 which is the insulating layer (12) is used as the bottom electrod Thereafter, cr the photo-resistor (18) spin is coated and the bottom electrode (11) is patterned through the etching process of developing are that as shown in the figure, the cathode electrode (11) is formed the wet etching is used and Nb performs RIE in CF4 and O2 mixed gas atmosphere.

As shown in Figure 4c, an oxide or a nitride is used as the insulating layer (12) after forming the botton SiO2 is deposited by the reactive sputtering or the low pressure chemical vapor deposition (LPCVD) in device to 0.5~5㎛ thickness. Thereafter, it may be acceptable that the Nb, which is the aluminium (Al) f oxidation and gate electrode material to the series processing Ti, W etc. are deposited. The same mate electrode (11) which is the bottom electrode is used. In order to form the fine hole (24) on the desired p Figure 4d, the photo-resistor (18) spin is coated and a pattern is formed into an exposure and the etchi developed. Here, or the mask for the resistant layer is used as the mask forming one pixel. Next, as sh the nanohole (24) is formed if it oxidizes. It has the anodic oxidized alumina (15) having the fine hole (2 the photo-resistor (18) as the hard mask and the anisotropic dry etching is performed. Off-taste, this is end of etching layer (etch stop layer) because it has *** (Cr) on the cathode electrode (11). Thereafter, (15) is performed a wet etching and it removes, the cavity (25) of a shape as illustrated in Figure 4g is time, the size of the cavity (25) coincides with the size of the anodic oxidized alumina fine hole (24). Ne forming pattern of the gate electrode (13) for the address drive which is not illustrated is performed. Tl formation method is identical with the cathode patterning method. And the pixel shape which is a final s

Figs. 5a through 5c are the cross-sectional view showing the field emission device of 3 electrode struc a preferred embodiment of the present invention.

As shown in Figure 5a, the process of forming the micro tip of the field emission device of a triode of th is same as those of the conventional tip-like shape pass gad if the sacrificial layer is after the slope cor off (lift-off) in order not to be evaporated inside the gate hole (24) after performing the perpendicularit evaporation the metal tip which is the emitter (23) material, the metal tip which is the emitter (23) can b diameter of the gate hole (24) is about hundreds ~ thousands Å and it thus fits and the height of the ga (12) is controlled.

As shown in Figure 5b, the process for selectively growing the carbon nanotube (17) of the field emissi CNT of a triode deposits the catalyzing transition metal (16) on the insulating layer (12) base part in wh hole by an electroplating. The cathode electrode (11) is to a cathode and Co electro is deposited on the electrode (11) which is in the insulating layer base part to about 1~10nm thickness. In the fine hole bas the carbon nanotube (17) has the catalyst metal, the carbon nanotube (17) selectively grows. If it spills which is the fuel gas after charging a specimen inside a reactor and maintaining the reactor temperature 600~900℃ range, the carbon nanotube (17) begins to grow in the catalyst metal (16) which is in the fin The last height controls this by the growth time to highly grow to immediately, the lower part with the g (13). In this way, the lower plate which is a final is manufactured.

As shown in Figure 5c, the size of the fine hole is small and the size is used as the structure of filling in inside oxidizing and is formed with a metal as the emitter (23). If the cathode bottom electrode (11) is t vapor deposits to the method for filling up a metal as an electroplating, the sharp metal can be formed v process. There can be the cr, ta, mo, ti, ni, co etc having strong the heat resistance as the metal which

Figure 6 shows the representative schematic diagram corresponding to an int-pixel of the present inve

Figure 7 shows the cross-sectional view of a pixel steal in fig. 6 according to the line "A-A'".

If figs. 6 and 7 are connected and it illustrates, the cathode electrode (11) and gate electrode (13) are c and it is formed and it is able to address. And the resistant layer (19) is classified into 4 domain within a is designed for the moreover uniform electron emission rather than. Therefore, the other part suppleme domain is destroyed the arcing etc. That is, the resistant layer (19) can be designed in one pixel to one In a this, as well as, the gate electrode (13), the gate hole (24) is formed and it corresponds to each gat the emitter (23) is formed on the cathode electrode (11). If the cathode electrode (11) formed in this wa potential and a voltage is authorized in the gate electrode (13), the high field hangs on the peak of emitt in the part in which two electrodes (11,13) intersect and the electronics is released with such high field voltage of the gate electrode (13) in which the electronics is released is decreased as the size of the ga becomes smaller. And it is changed according to the material characteristic of the emitter (23).

Referring to Figure 8, the upper plate (27), an e-source including the metal tip, the catalyst metal (16) a nanotube (17) etc, and the lower plate (10) are included. As to the upper plate (27), the anode electrode fluorescent substance (22) are laminated. As to the lower plate (10), the cathode electrode, the resistan the gate electrode formed on the resistant layer (19), and the insulating layer formed on the gate electr Moreover, the spacer (20) for enduring the vacuum stress with maintaining a gap between the upper pla lower glass substrate (10) on the lower plate (10) in the upper plate (27) and sealing is formed.

The upper plate (27) coats with the fluorescent substance of the respective 3 kinds after patterning and transparent electrode on the glass substrates. By radiating the fluorescent substance (22) in which elec released from emitter (23) of the spot in which two electrodes (11,13) intersect and facing by successiv voltage in cathode electrode (11) and gate electrode (13), each pixel is successively radiated. In the an in which the fluorescent substance (22) is coated onto, it collides with the fluorescent substance (22) in pressure is applied and which accelerates the electronics emitted in the emitter (23) and corresponding

At this time, as to a luminance and color embodying of the individual pixel, the color embodying become through the red (R), which is adjacent while controlling a luminance by using the principles that the curr emitted by the voltage difference which hangs between the emitter (23) and gate electrode (13) is chan and the brightness control of the T'ien-Ch'ih pixel of the blue (B).

Effect of Invention(Device)

As described above, as to the field emission device, while since controlling the size and density of a mi the anodic oxidation process, controlling the density of the carbon nanotube and the emission current, a possible through the thin film deposition and anodic oxidation process.

Moreover, as to this anodic oxidation process, while applying to the gate hole formation process of the device of the conventional tip shape and controlling the emission current to the driving voltage lower th easily controls the gate hole size by the anodic oxidation process to 10nm.

As illustrated in the above, it will be able to know at the range that does not deviate from the technical present invention if it is the person skilled in the art that a change and the various correction are possit technical scope of the present invention is not restricted to the content that is written in the detailed de specification but it determines by the range of the patent claim.

Scope of Claim(s)

Claim [1]

The method of manufacturing a gate hole of the field emission device comprising: the step laminating tl and metal layer onto the top of the substrate, the step oxidizing the metal layer and forms a plurality o the metal layer, and the step that forms a cavity on the insulating layer by having the anodic oxidized n mask and removing the insulating layer between the metal pattern.

Claim [2]

The method of manufacturing a gate hole of the field emission device of claim 1, wherein the material uses the aluminium (Al).

Claim [3]

The field emission device comprising: a plurality of fine holes which is formed with an anodizing and pl laminates the insulating layer and metal layer onto the top of the substrate and the emitter which emits is positioned within the fine hole and the lower plate including the gate electrode drawing out the elect emitter and the upper plate, including the transparent electrode and fluorescent substance and the spac maintains the vacuum gap of the lower plate and top it is formed on the upper plate done.

Claim [4]

The field emission device of claim 3, wherein the material of the metal layer uses the aluminium (Al).

Claim [5]

The field emission device of claim 3, wherein the material of an emitter is one among the carbon nanot

Claim [6]

The field emission device of claim 4, wherein the side in which the emitter electronics is released is th

Claim [7]

The field emission device of claim 4, wherein the side in which the emitter electronics is released is th

Claim [8]

The manufacturing method of the field emission device comprising: a plurality of fine holes which is fo anodizing and photo etching it laminates the insulating layer and metal layer onto the top of the substra which emits the electronics it is positioned within the fine hole and the step including the gate electrod electronics from an emitter in the lower plate and the step, that includes the transparent electrode and substance in the upper plate and the step that is formed on the upper plate and maintains the vacuum g plate and top with a spacer.

Claim [9]

The manufacturing method of the field emission device of claim 8, wherein the material of the metal la aluminium (Al).

Claim [10]

The manufacturing method of the field emission device of claim 8, wherein the material of an emitter is carbon nanotube and metal.

Claim [11]

The manufacturing method of the field emission device of claim 10, wherein the side in which the emitt released is the plane.

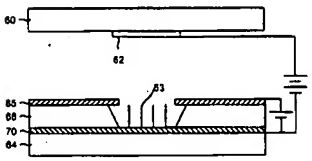
Claim [12]

The manufacturing method of the field emission device of claim 10, wherein the side in which the emitt released is the conical shape.

Drawing

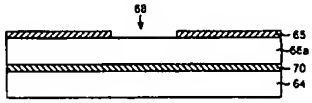
Drawing(s)

Drawing1

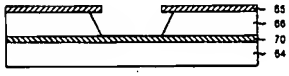


Drawing2a

Drawing2b



Drawing2c



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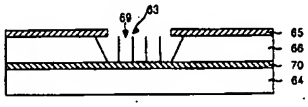

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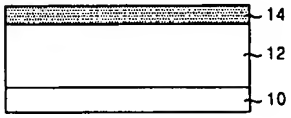
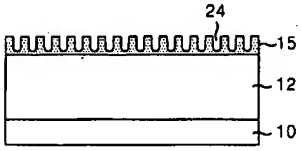
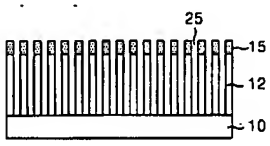


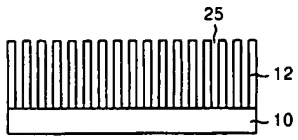
Drawing3b

Drawing3c

Drawing3d





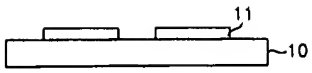


Drawing4a

Drawing4b

Drawing4c

Drawing4d



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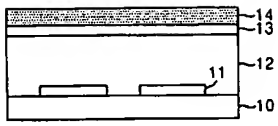

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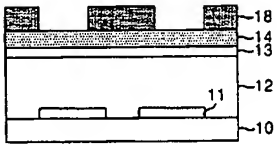
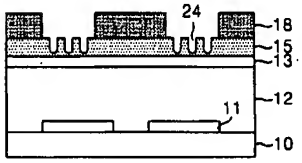
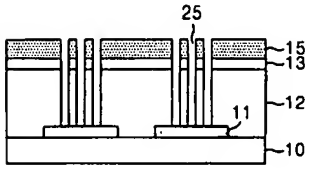


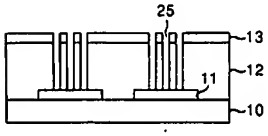
Drawing4g



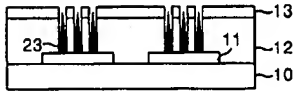
Drawing5a



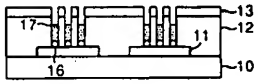
Drawing5b



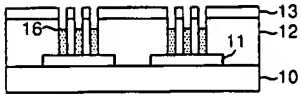
Drawing5c



Drawing6



Drawing7



Drawing8